



# STD3LN62K3, STF3LN62K3 STP3LN62K3, STU3LN62K3

N-channel 620 V, 2.5  $\Omega$ , 2.5 A SuperMESH3™ Power MOSFET  
DPAK, TO-220FP, TO-220, IPAK

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>D</sub>
STD3LN62K3	620 V	< 3 $\Omega$	2.5 A	45 W
STF3LN62K3			2.5 A <sup>(1)</sup>	20 W
STP3LN62K3			2.5 A	45 W
STU3LN62K3			2.5 A	45 W

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

## Application

Switching applications

## Description

These devices are made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

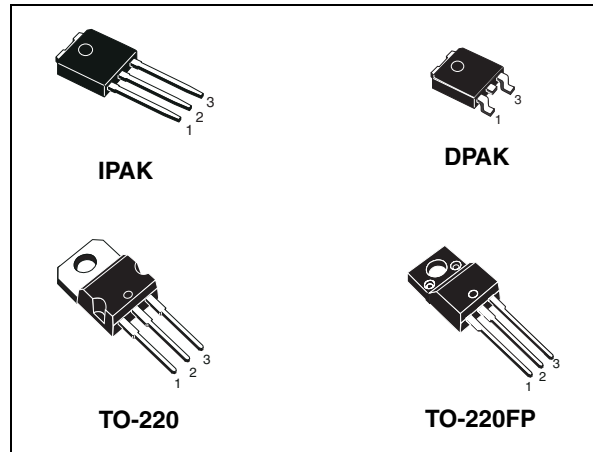


Figure 1. Internal schematic diagram

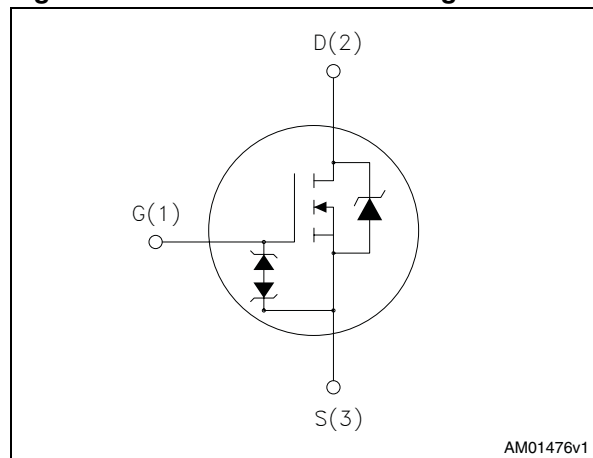


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD3LN62K3	3LN62K3	DPAK	Tape and reel
STF3LN62K3		TO-220FP	Tube
STP3LN62K3		TO-220	
STU3LN62K3		IPAK	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		TO-220	DPAK IPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	620			V
$V_{GS}$	Gate- source voltage	$\pm 30$			V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.5		2.5 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.6		1.6 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	10		10 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45		20	W
	Derating factor	0.36		0.16	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100 pF, R = 1.5 kΩ)	2500			V
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	12			V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ }^\circ\text{C}$ )	2500			V
$T_{stg}$	Storage temperature	-55 to 150			°C
$T_j$	Max. operating junction temperature	150			°C

- Limited by package
- Pulse width limited by safe operating area
- $I_{SD} \leq 2.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ , peak  $V_{DS} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	TO-220	DPAK IPAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.78		6.25	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max		50		°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		62.5	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300		300	°C

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	90	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	620			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.25\text{ A}$		2.5	3	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	386	-	pF
$C_{oss}$	Output capacitance			30		pF
$C_{rss}$	Reverse transfer capacitance			5		pF
$C_{o(tr)}^{(1)}$	Eq. capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }496\text{ V}$	-	20	-	pF
$C_{o(er)}^{(2)}$	Eq. capacitance energy related			28		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 496\text{ V}$ , $I_D = 2.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	17	-	nC
$Q_{gs}$	Gate-source charge			2.7		nC
$Q_{gd}$	Gate-drain charge			10.7		nC

1.  $C_{oss\text{ eq.}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

2.  $C_{oss\text{ eq.}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$ , $I_D = 1.25\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> )		9		ns
$t_r$	Rise time			7		ns
$t_{d(off)}$	Turn-off-delay time			30	-	ns
$t_f$	Fall time			27		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				10	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.5\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 24</a> )	-	240		ns
$Q_{rr}$	Reverse recovery charge			1200		nC
$I_{RRM}$	Reverse recovery current			10		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 24</a> )	-	265		ns
$Q_{rr}$	Reverse recovery charge			1400		nC
$I_{RRM}$	Reverse recovery current			11		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 9. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30	-		V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

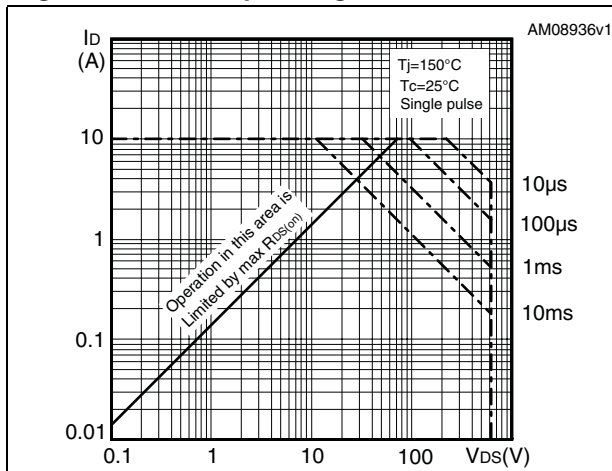


Figure 3. Thermal impedance for TO-220

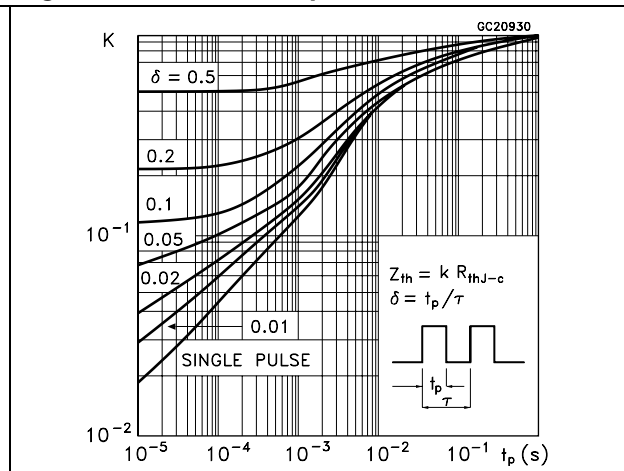


Figure 4. Safe operating area for TO-220FP

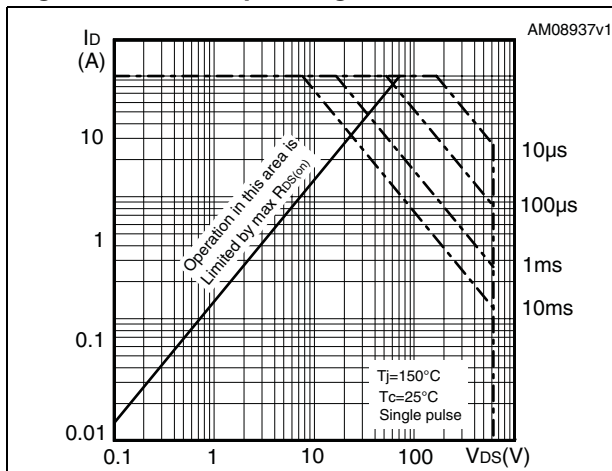


Figure 5. Thermal impedance for TO-220FP

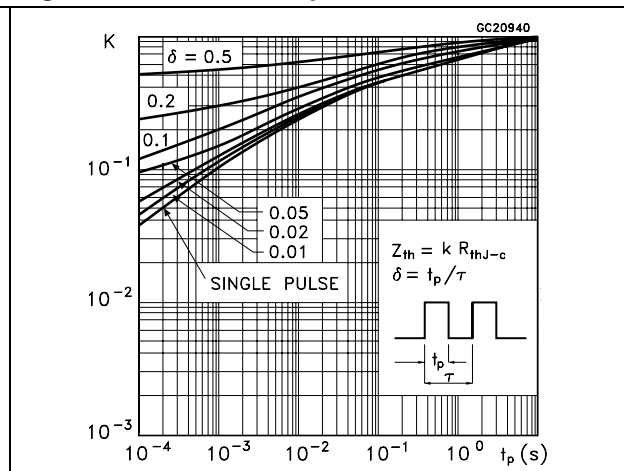


Figure 6. Safe operating area for DPAK, IPAK

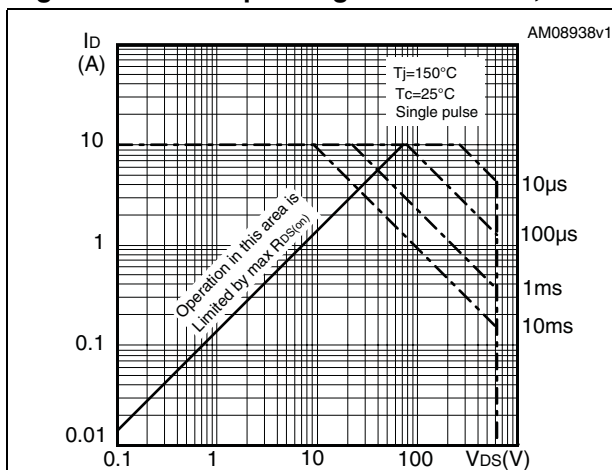


Figure 7. Thermal impedance for DPAK, IPAK

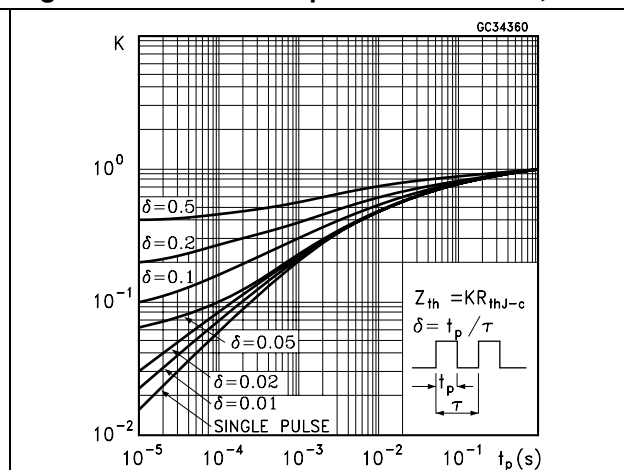


Figure 8. Output characteristics

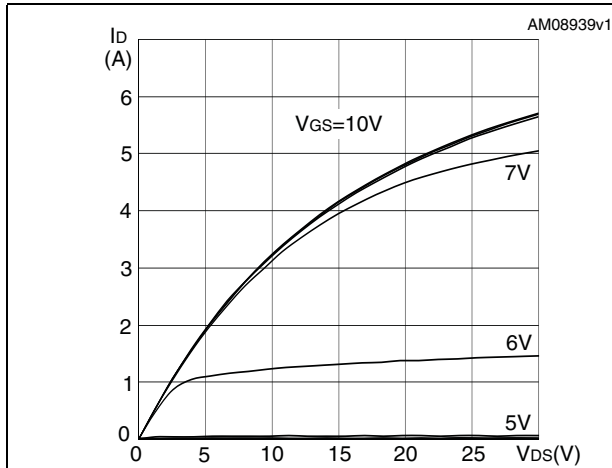


Figure 9. Transfer characteristics

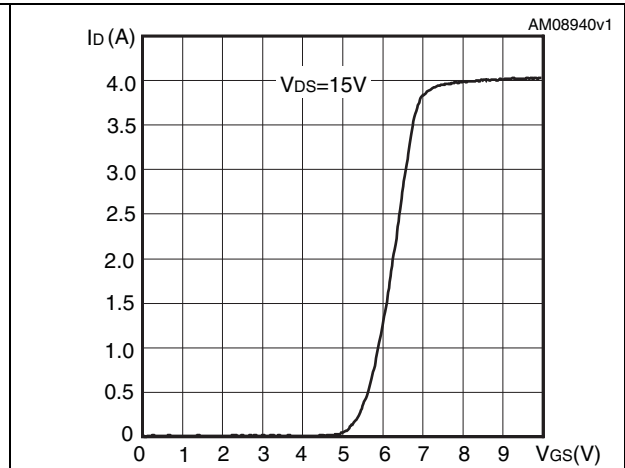


Figure 10. Gate charge vs gate-source voltage

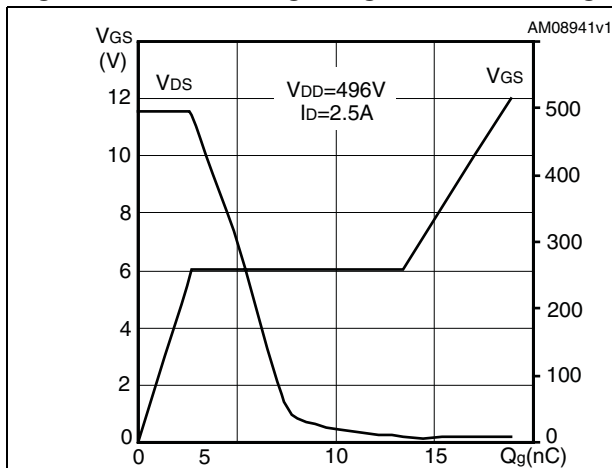


Figure 11. Static drain-source on resistance

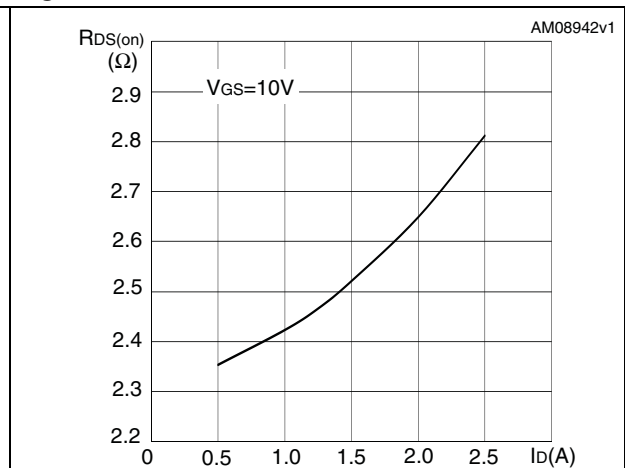


Figure 12. Capacitance variations

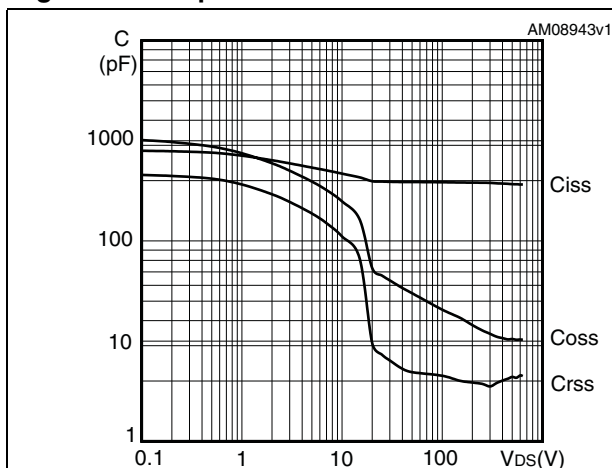


Figure 13. Output capacitance stored energy

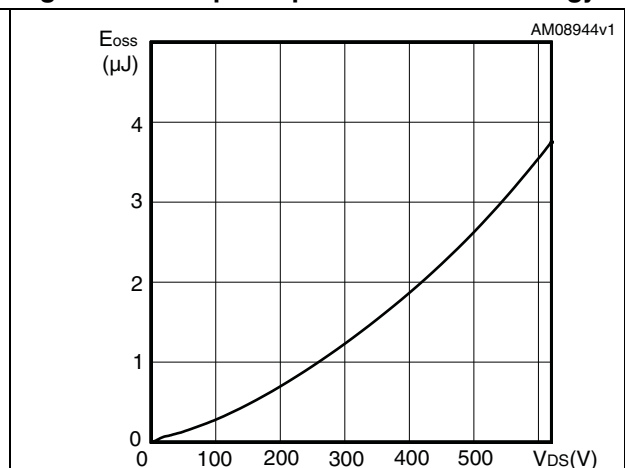


Figure 14. Normalized gate threshold voltage vs temperature

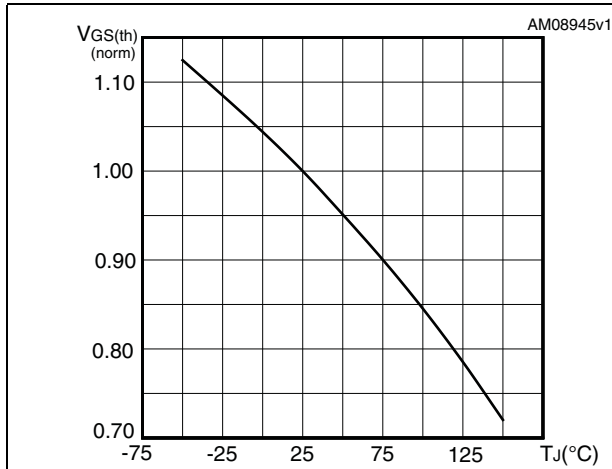


Figure 15. Normalized on resistance vs temperature

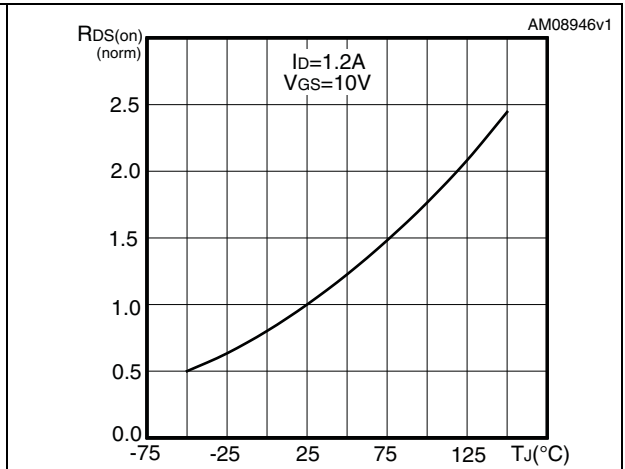


Figure 16. Normalized BV<sub>DSS</sub> vs temperature

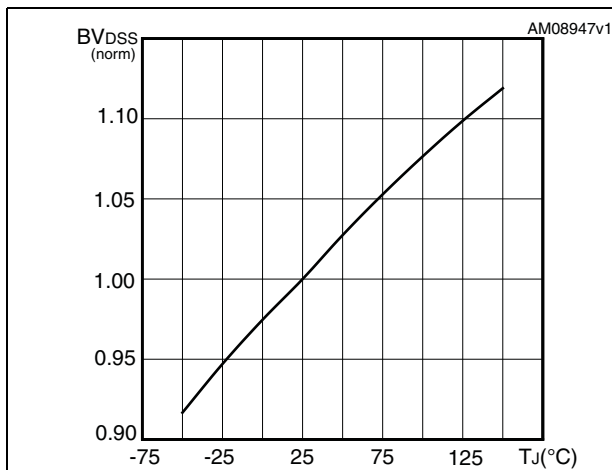


Figure 17. Source-drain diode forward characteristics

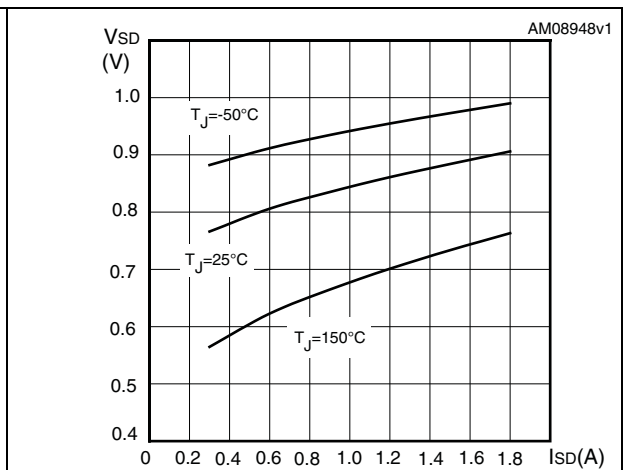
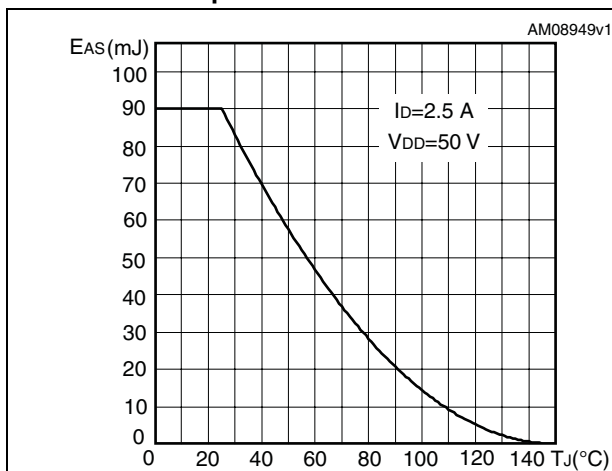


Figure 18. Maximum avalanche energy vs temperature





### 3 Test circuits

**Figure 19. Switching times test circuit for resistive load**



AM01468v1

**Figure 20. Gate charge test circuit**



AM01469v1

**Figure 21. Test circuit for inductive load switching and diode recovery times**



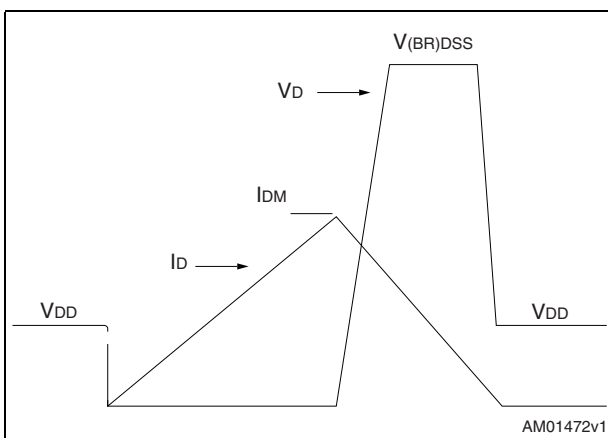
AM01470v1

**Figure 22. Unclamped Inductive load test circuit**



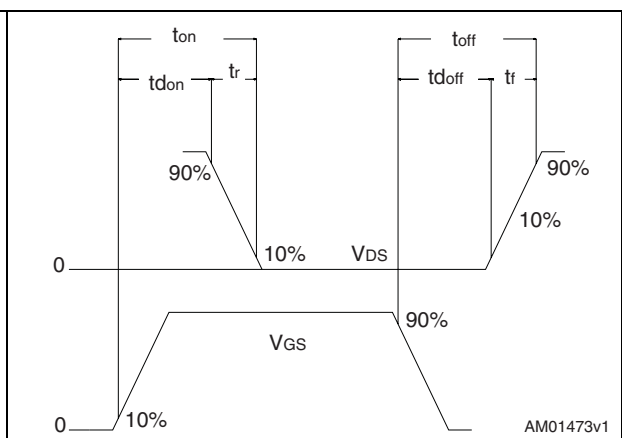
AM01471v1

**Figure 23. Unclamped inductive waveform**



AM01472v1

**Figure 24. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

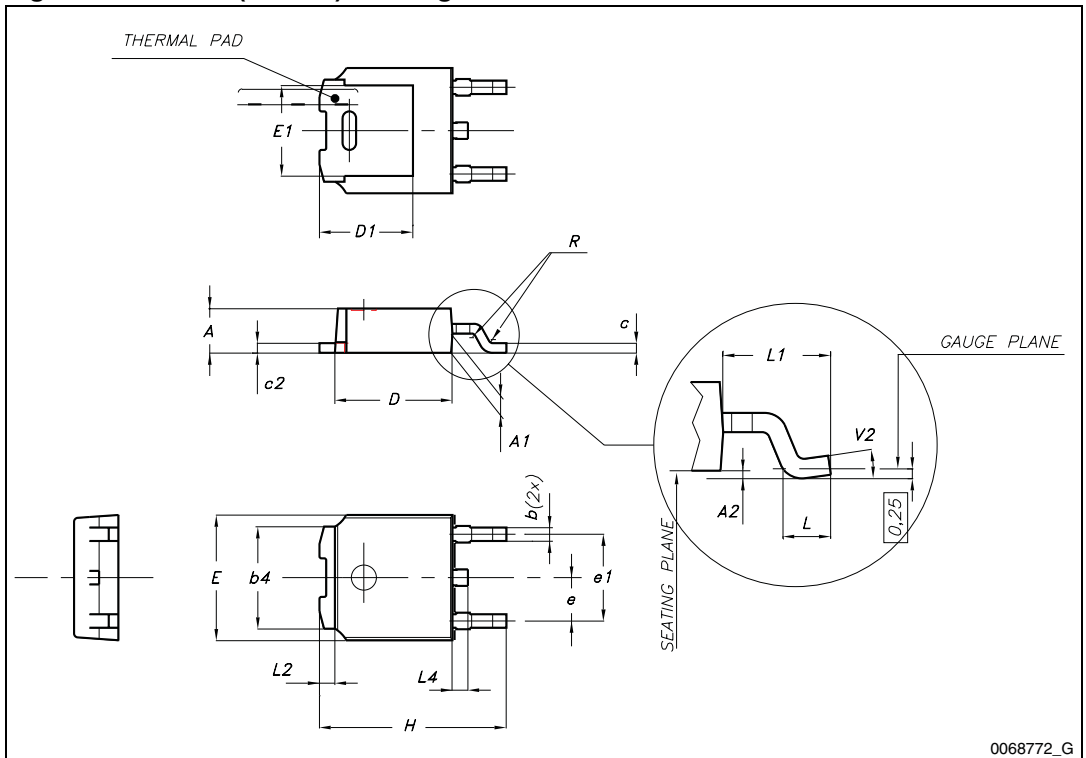


Table 11. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 26. IPAK (TO-251) drawing

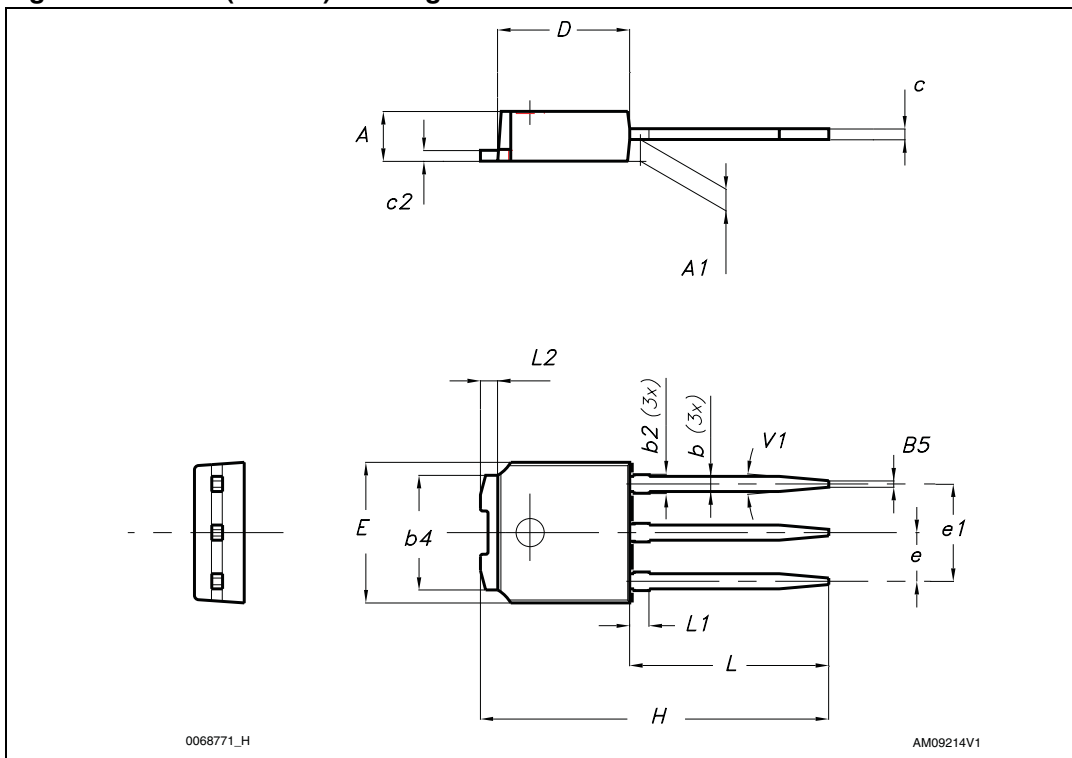
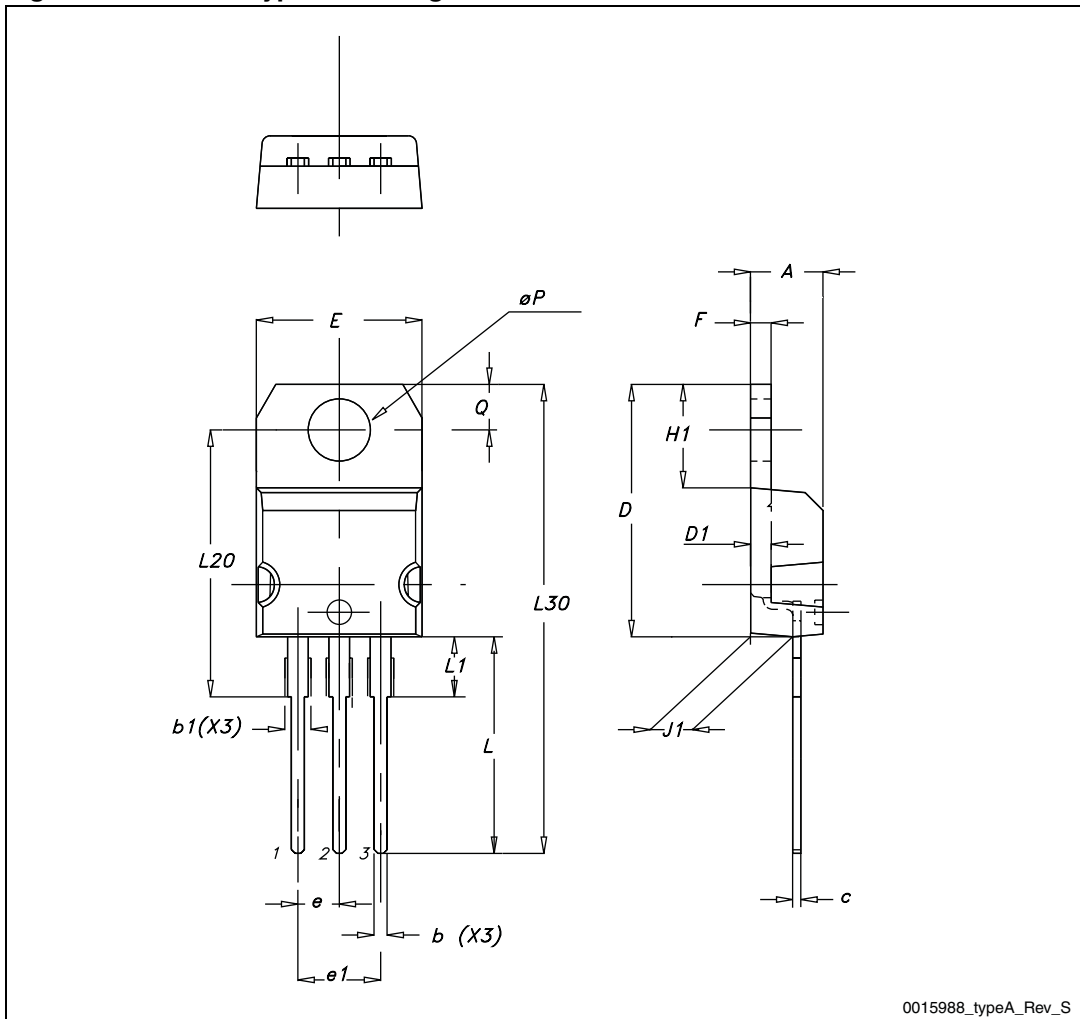


Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing



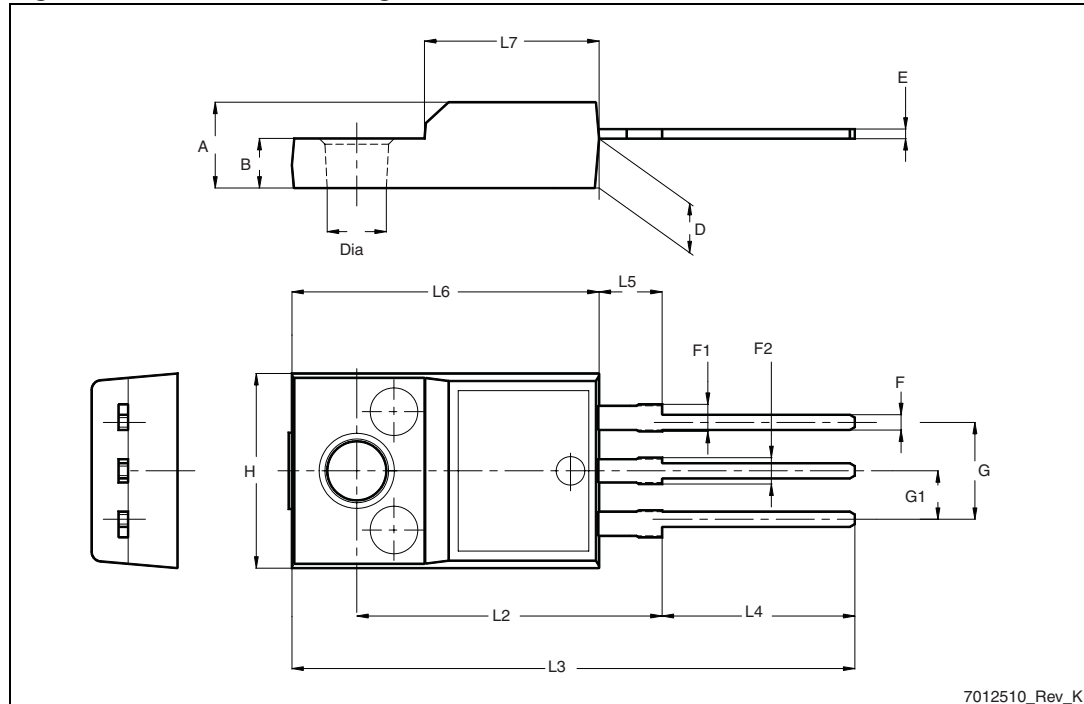
0015988\_typeA\_Rev\_S



Table 13. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 28. TO-220FP drawing



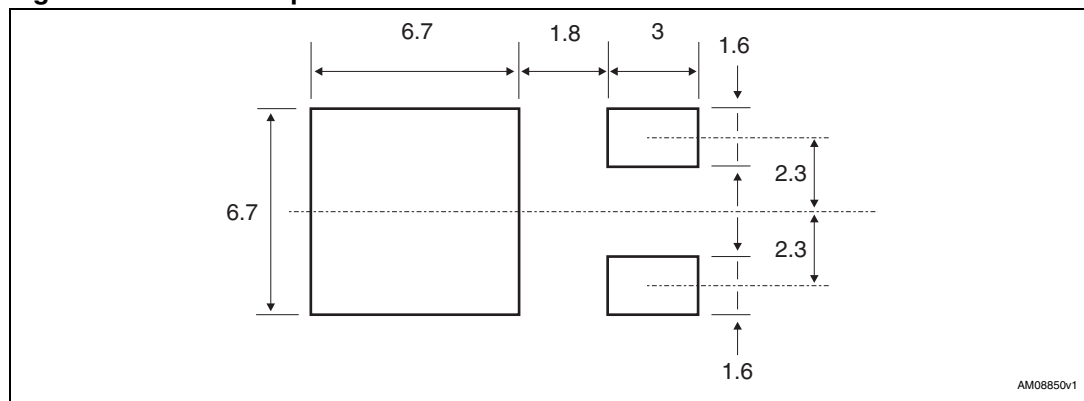
7012510\_Rev\_K

## 5 Packaging mechanical data

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.	2500	
P1	7.9	8.1	Bulk qty.	2500	
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 29. DPAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Figure 30. Tape for DPAK (TO-252)

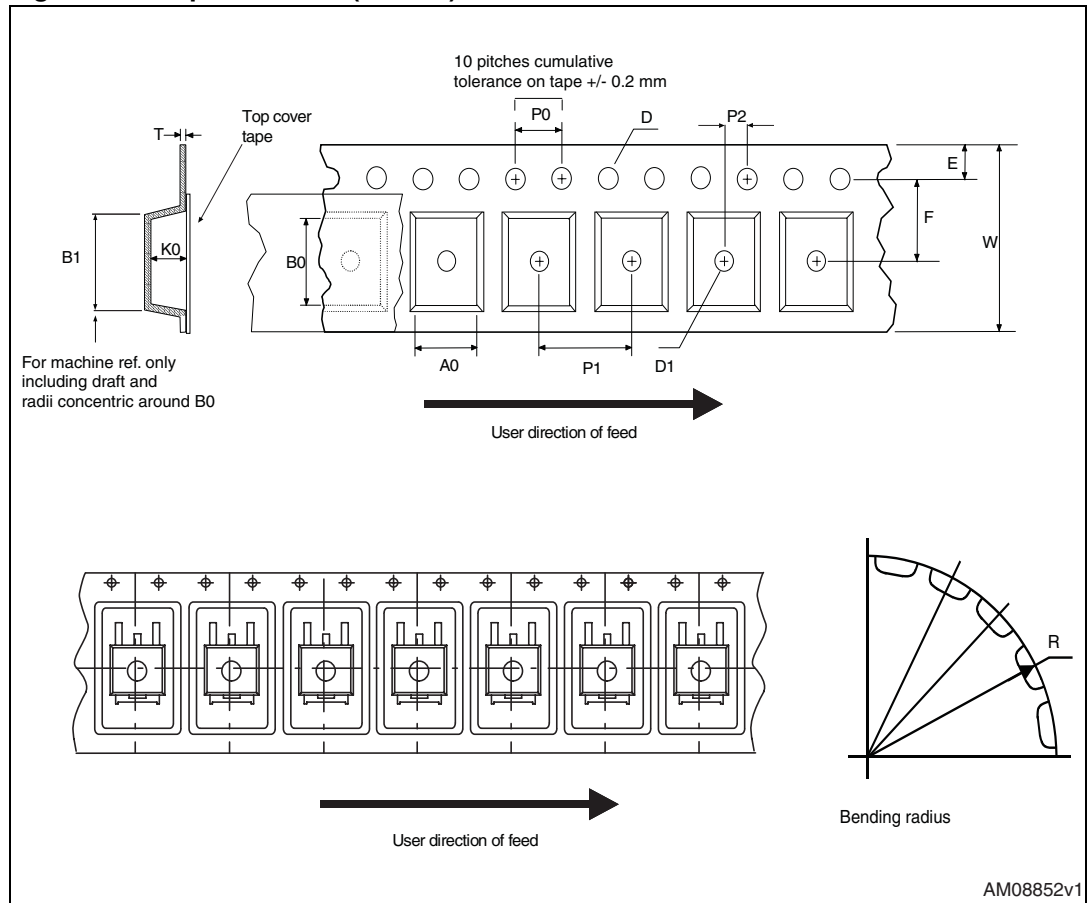
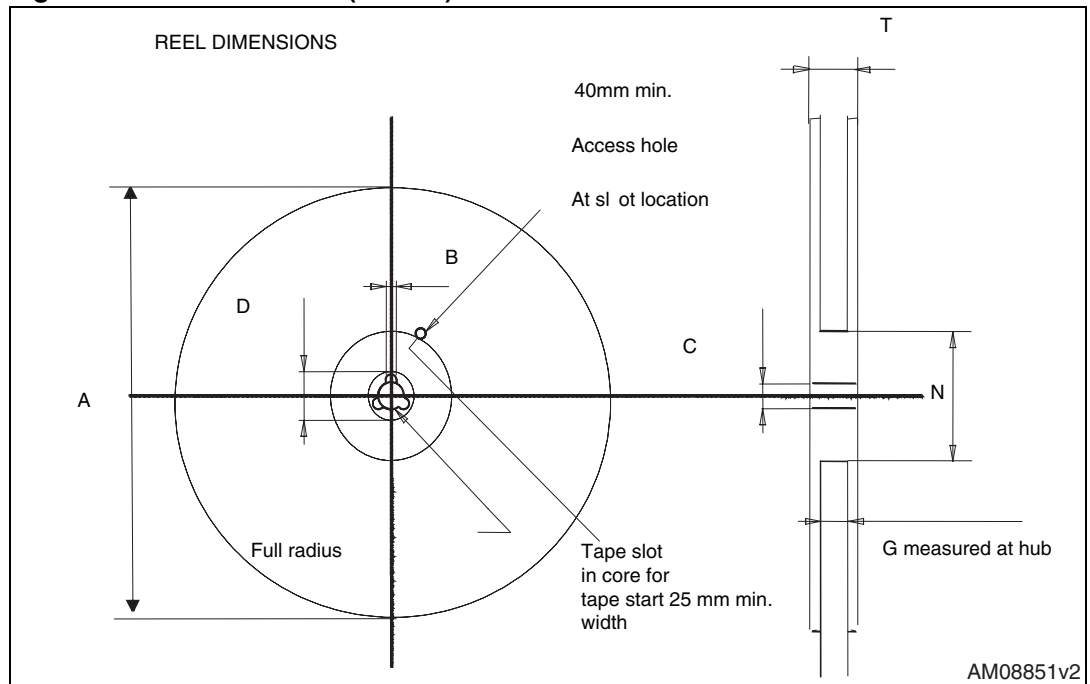


Figure 31. Reel for DPAK (TO-252)



## 6 Revision history

Table 15. Document revision history

Date	Revision	Changes
04-Feb-2011	1	First release.

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